MEMORY WITH MULTIPLE STATE CELLS AND SENSING METHOD

Abstract of the Disclosure

A memory has an array made up of transistors that have two charge storage regions between the channel and control gate. Each bit is made up of two charge storage regions that are from different transistors. A bit is written by first erasing all of the storage locations and then writing one of the charge storage locations that make up the bit. A pair of charge storage locations, one erased and the other programmed, is identified for each bit. The logic state of the bit is read by comparing the charge stored in the two charge storage locations that make up the bit. This comparison is achieved by generating signals representative of the charge present in the two charge storage locations. These signals are then coupled to a sense amplifier that functions as a comparator. This avoids many problems that accompany comparisons to a fixed reference.